INSTITUTO POLITÉCNICO DE BRAGANÇA

Course Unit	Computer Architecture			Field of study	Computer Engineering		
Bachelor in	Informatics Engineering			School	School of Technology and Management		
Academic Year	2023/2024	Year of study	1	Level	1-1	ECTS credits	6.0
Type	Semestral	Semester	2	Code	9119-706-1201-00-23		

Workload (hours)	162	Contact hours	T	TP	PL	TC	S	E	OT	O
			30	-	30	-	-	-	-	-

T - Lectures; TP - Lectures and problem-solving; PL - Problem-solving, project or laboratory; TC - Fieldwork; S - Seminar; E - Placement; OT - Tutorial; O - Other

Name(s) of lecturer(s): José Carlos Rufino Amaro, ARNALDO ANTÓNIO PINTO PEREIRA, Gilberto Sousa Ferraz

Learning outcomes and competences

At the end of the course unit the learner is expected to be able to:
1. understand the role of each computing system component
2. know the operating mechanism of a processor and its interaction with the other system components
3. understand the effect produced by high-level programming languages code fragments at the level of computing systems hardware
4. predict the impact that a specific hardware upgrade would produce in the entire system performance
5. size and evaluate computing systems

Prerequisites

Before the course unit the learner is expected to be able to:
1. know the role of digital logic in the context of computing systems
2. understand the operation and the goal of small programmes written in C language

Course contents

Introduction to computer architecture and organization. Data representation. MARIE simplified architecture. Instruction set architectures. Memory. Input/Output and storage systems. Performance measurement and optimization. Alternative architectures.

Course contents (extended version)

1. Introduction to computer architecture and organization
   - SI and IEC units of measurement
   - main components of a computer
   - standards organizations
   - historical evolution
   - the computer level hierarchy
   - the von Neumann model
2. Data representation
   - positional numbering systems
   - conversion between different number bases
   - signed integer representation
   - floating-point representation
   - character codes
   - error detection and correction
3. Study of a simulated architecture
   - basic components of a CPU
   - basic organization of the Main Memory
   - MARIE CPU structure and organization
   - MARIE instruction set architecture
   - MARIE instruction processing
   - MARIE assembly programs
   - MARIE instructions decoding
4. Instruction set architectures
   - instruction formats
   - instruction types
   - addressing
   - instruction-level pipelining
   - CISC vs RISC
5. Memory
   - types of memory
   - the memory hierarchy
   - main memory
   - cache memory
   - virtual memory
6. Input/Output and storage systems
   - buses
   - I/O subsystem
   - I/O architectures
   - storage technologies
   - RAID schemes
7. Performance measurement and optimization
   - mathematical metrics
   - benchmarking
   - CPU performance optimization
   - Amdahl's law
8. Alternative architectures
   - Flynn's taxonomy
   - parallel systems
   - other systems

Recommended reading

1. "The essentials of computer organization and architecture, 5th Ed. "; Linda Null, Julia Lobur; Jones and Bartlett Publishers; 2018
2. "Princípios Básicos de Arquitetura e Organização de Computadores, 2ª Edição"; Linda Null, Julia Lobur; Bookman; 2010
3. "Arquitectura de Computadores, 5ª Edição"; José Delgado, Carlos Ribeiro; FCA; 2014

Recommended reading

4. "Computer Organization and Design: The Hardware/Software Interface, 5th Revised Ed. "; D. A. Patterson, J. L. Hennessy; Morgan Kaufman; 2013
5. "Computer Architecture: A Quantitative Approach, 6th Ed. "; J. L. Hennessy, D. A. Patterson; Morgan Kaufman; 2017

Teaching and learning methods

The subject is taught by interleaving the exposition of theoretical concepts with the resolution of exercises. All documentation (slides, exercises, solutions) is provided through the IPB e-learning platform.

Assessment methods

1. Alternative 1 - (Regular, Student Worker) (Final)
   - Intermediate Written Test - 40% (first intermediate test (part P1))
   - Intermediate Written Test - 40% (second intermediate test (part P2))
   - Final Written Exam - 20% (first oficial exam (part P3))
2. Alternative 2 - (Regular, Student Worker) (Supplementary)
   - Final Written Exam - 100% (second oficial exam (structured in parts P1, P2 and P3; allows evaluation of any part combination))
3. Alternative 3 - (Regular, Student Worker) (Special)
   - Final Written Exam - 100% (exam with the same structure of the 2nd oficial exam and reuse of the previous grades of the 3 parts)

Language of instruction

1. Portuguese
2. English

Electronic validation

José Carlos Rufino Amaro	Tiago Miguel Ferreira Guimaraes Pedrosa	Luís Manuel Alves	Nuno Adriano Baptista Ribeiro
23-02-2024	14-03-2024	16-03-2024	17-04-2024