INSTITUTO POLITÉCNICO DE BRAGANÇA

Course Unit	Computer Architecture			Field of study	Computer Engineering		
Bachelor in	Informatics Engineering			School	School of Technology and Management		
Academic Year	2021/2022	Year of study	1	Level	1-1	ECTS credits	6.0
Type	Semestral	Semester	2	Code	9119-706-1201-00-21		

Workload (hours)	162	Contact hours	T	TP	PL	TC	S	E	OT	O
			30	-	30	-	-	-	-	-

T - Lectures; TP - Lectures and problem-solving; PL - Problem-solving, project or laboratory; TC - Fieldwork; S - Seminar; E - Placement; OT - Tutorial; O - Other

Name(s) of lecturer(s): José Carlos Rufino Amaro, Antonio Jose Moreira de Carvalho, Gilberto Sousa Ferraz

Learning outcomes and competences

At the end of the course unit the learner is expected to be able to:
1. understand the role of each computing system component
2. know the operating mechanism of a processor and its interaction with the other system components
3. understand the effect produced by high-level programming languages code fragments at the level of computing systems hardware
4. predict the impact that a specific hardware upgrade would produce in the entire system performance
5. size and evaluate computing systems

Prerequisites

Before the course unit the learner is expected to be able to:
1. know the role of digital logic in the context of computing systems
2. understand the operation and the goal of small programmes written in C language

Course contents

Introduction to computer architecture and organization. Floating-point representation. Study of a simulated architecture. Instruction set architectures. Memory. Input/Output and storage systems. Alternative architectures. Performance evaluation and benchmarking.

Course contents (extended version)

1. Introduction to computer architecture and organization
   - main components of a computer
   - historical evolution
   - the computer level hierarchy
   - the von Neumann model
2. Floating-point representation
   - simplified representation model
   - floating point arithmetic
   - floating point errors
   - IEEE-754 standard
3. Study of a simulated architecture
   - CPU structure and organization
   - buses and clocks
   - I/O subsystem
   - memory organization and addressing
   - instruction set architecture
   - instruction processing
   - assembly programs
   - simulation tools
4. Instruction set architectures
   - instruction formats
   - instruction types
   - addressing
   - instruction-level pipelining
5. Memory
   - types of memory
   - the memory hierarchy
   - cache memory
   - virtual memory
6. Input/Output and storage systems
   - Amdahl's law
   - I/O architectures
   - storage technologies
7. Alternative architectures
   - RISC machines
   - Flynn's taxonomy
   - parallel systems
8. Performance evaluation and benchmarking
   - mathematical metrics
   - benchmarking
   - CPU performance optimization

Recommended reading

1. "The essentials of computer organization and architecture, 5th Ed. "; Linda Null, Julia Lobur; Jones and Bartlett Publishers; 2018
2. "Princípios Básicos de Arquitetura e Organização de Computadores, 2ª Edição"; Linda Null, Julia Lobur; Bookman; 2010
3. "Arquitectura de Computadores, 5ª Edição"; José Delgado, Carlos Ribeiro; FCA; 2014
4. "Computer Organization and Design: The Hardware/Software Interface, 5th Revised Ed. "; D. A. Patterson, J. L. Hennessy; Morgan Kaufman; 2013
5. "Computer Architecture: A Quantitative Approach, 6th Ed. "; J. L. Hennessy, D. A. Patterson; Morgan Kaufman; 2017

Teaching and learning methods

The subject is taught by interleaving the exposition of theoretical concepts with the resolution of exercises. This is complemented by practical questions to be solved outside classes. All documentation (slides, exercises, solutions) is provided through the IPB e-learning platform.

Assessment methods

1. Alternative 1 - (Regular, Student Worker) (Final)
   - Intermediate Written Test - 25% (first intermediate test (part T1))
   - Intermediate Written Test - 25% (second intermediate test (part t2))
   - Final Written Exam - 50% (final exam (part T3))
2. Alternative 2 - (Regular, Student Worker) (Supplementary)
   - Final Written Exam - 100% (last resource exam (structured in parts T1, T2, T3; allows evaluation of any part combination))
3. Alternative 3 - (Regular, Student Worker) (Special)
   - Final Written Exam - 100% (exam on all topics subject to evaluation, without reusing any previous grades)

Language of instruction

Portuguese

Electronic validation

José Carlos Rufino Amaro	José Luís Padrão Exposto	Luísa Maria Garcia Jorge	Paulo Alexandre Vara Alves
09-06-2022	05-07-2022	07-07-2022	07-07-2022