

Course Unit	Digital Electronics	Field of study	Computer Engineering
Bachelor in	Informatics Engineering	School	School of Technology and Management
Academic Year	2023/2024	Year of study	1
Type	Semestral	Semester	1
Workload (hours)	162	Contact hours	T - 60 TP - 60 PL - TC - S - E - OT - O -
		Level	1-1
		ECTS credits	6.0
		Code	9119-706-1105-00-23

T - Lectures; TP - Lectures and problem-solving; PL - Problem-solving, project or laboratory; TC - Fieldwork; S - Seminar; E - Placement; OT - Tutorial; O - Other

Name(s) of lecturer(s) Getúlio Paulo Peixoto Igrejas, Adriano Manuel Alves Ferreira, Andre Chaves Mendes, Gustavo Silva Funchal, Joao Afonso Braun Neto, Luis Fernando Piardi

Learning outcomes and competences

At the end of the course unit the learner is expected to be able to:

1. Simplify logical functions using both analytical and graphical methods.
2. Know the principal electrical characteristics of the TTL and CMOS family.
3. Design application specific combinatory digital circuits.
4. Design counters for non-monotonic and non-consecutive sequences.
5. Design MIMO sequential machines.
6. Understand the structure and operation of electronic memories and digital programming devices.
7. Be able to write simple programs for the ARDUINO development platform.

Prerequisites

Before the course unit the learner is expected to be able to:
Not applicable.

Course contents

Number Systems and Binary Codes. Logic Gates and Boolean Algebra. Logical Operations using electrical signals. Combinatory Integrated Circuits. Sequential Logic Circuits. Development of programs for the ARDUINO platform.

Course contents (extended version)

1. Number Systems and Binary Codes
 - Conversion between the binary, octal and hexadecimal number system
 - Signed Number Representation
 - Arithmetic Operations
 - Binary Codes
 - Introduction to data transmission
2. Logic Gates and Boolean Algebra
 - Boolean Variables
 - Elementary Logic Operations
 - Canonical form of a logical expression
 - Other logical operations
 - Logical Gates and Logical diagrams
 - The NAND and NOR functions as universal modelling operators
 - Theorems and properties of Boole's Algebra
 - Logical Expression Simplification
3. Logical Operations using electrical signals
 - Logical Integrated Circuits (IC)
 - Logical IC Families
 - Switching Dynamics
4. Combinatory Integrated Circuits
 - Coders and decoders
 - Multiplexers and Demultiplexers
 - Logical function modelling using multiplexers
 - Code converters
 - Adders, subtractors and ALU's
5. Sequential Logic Circuits
 - Multivibrators
 - Latches and Flip-Flop's
 - Counters
 - Counters Design method
 - Registries
 - Integrated Circuits
 - State Machine
 - Synchronous Sequential Circuits
6. Introduction to microprocessors and microcontrollers
 - ARDUINO platform architecture
 - Input/Output ports
 - Microcontroller programming
 - Flow control instructions
 - Cycle instructions

Recommended reading

1. Digital Electronics – Tokheim, McGraw Hill, 2007
2. VHDL Programming by Example – D. Perry, Mc Graw Hill, 2002
3. Digital Design: Principles and Practices - John F. Wakerly, Prentice Hall, 2005

Teaching and learning methods

Most of the topics will be introduced, by the teacher, in presential classes. The concepts will be further investigated: - On presential sessions where the concepts are introduced and laboratory assignments are developed. - On non-presential time where the topics are further exploited by means of application exercises or group work assignments.

Assessment methods

1. Average of the laboratorial and final exams - (Regular, Student Worker) (Final, Supplementary, Special)
 - Laboratory Work - 60%
 - Final Written Exam - 40% (Mandatory to have a minimum of 7 on the final exam.)
2. The grade depends only on the final exam - (Regular, Student Worker) (Final, Supplementary, Special)
 - Final Written Exam - 100%

Language of instruction

1. Portuguese
2. English

Electronic validation

Getúlio Paulo Peixoto Igrejas	José Luís Sousa de Magalhaes Lima	Lúisa Maria Garcia Jorge	José Carlos Rufino Amaro
02-10-2023	11-10-2023	16-10-2023	31-10-2023